REMARKS

I. Claims

Claims 1-17 are pending in this application. Claims 1, 7, and 13 are independent.

II. Allowable Subject Matter

Applicants wish to thank the Examiner for indicating that claims 3-6, 11, 12, and 17 are allowable, and that claims 2 and 8-10 may be allowed.

III. Claim Rejection – 35 USC 112

Claims 1, 2, 7-10, 13, 15, and 16 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

The Office Action indicates that the word "kinds" is indefinite. The Office Action indicates that the phrases "said bit string" and "said smaller number of bits" lack proper antecedent basis. Accordingly, Applicants have amended claims 1-4, 7-10, 13, and 15-17. Applicants request reconsideration and withdrawal of the rejection.

IV. Claim Rejection – 35 USC 103

Claims 1 and 7 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art disclosed in the present application in view of U.S. Patent 6,147,963 ("Walker").

The rejection addresses the steps of claim 1 and states that the steps of:

inspecting the bit string in groups of the smaller number of bits, and thereby determining whether one of the control codes is present in the serial signal received on the transmission path is taught by the Encoder 110 (transforming 8 bits to 10 bits) and packet producing circuit 406 of the prior art shown in present Figure 1;

selecting the control code is taught by page 6, lines 31-33, which states

> "During the sending, control portion 405 determines the contents of the packet to be sent to the equipment on the opposite side as well as the timing of such sending based on the receive-control code"; and

sending the bit string containing at least one control code is taught by page 7, lines 1-5, which states

> "control portion 405 has a function of determining the control code to be sent to the packet producing circuit as well as a function of producing a send-enable signal for instructing the packet producing circuit whether the sending is to be performed or not."

The rejection relies on Walker (Figures 2 and 4) for teaching the remaining step of receiving the data code. Figures 2 and 4 show an encoder/decoder circuit.

V. Summary of the Present Invention

Claim 7, in a preferred embodiment, is directed to a transmission device for transmitting on a serial transmission path (e.g., transmission path 101) a data code encoded by superimposing a clock signal (data codes encoded by encoder 110) for decoding data to be transmitted, the encoded data code is of a predetermined first bit length (e.g., data code of 10 bits), the

transmission device using a plurality of control codes to be exchanged on the serial transmission path between a sender and a receiver side, each of the plurality of control codes is of a second bit length and having a smaller number of bits than the predetermined first bit length (e.g., control codes of 5 bits), the transmission device comprising:

determining means for inspecting the bit string in groups of bits of the second bit length in order to determine whether one of the plurality of control codes is present in the serial signal received on the serial transmission path or not (e.g. control portion 105 receiving a "receive-control code" 202 from character synchronizing circuit 104 and determines if the received code is the data start code 164 or not – see paragraph bridging pages 19-20),

sending means for determining the second control code to be sent based on a result of the determination of the determining means that a first control code is received, and sending a bit string containing at least the second control code to be sent onto the serial transmission path (e.g. sending "send-control packet" 210 by packet producing circuit 106 – page 20, lines 14-22),

data code receiving means for receiving the data code by inspecting the bit string in groups of bits of the first bit length in response to determination by the determining means that the first control code indicates the start of transmission of the data from the opposite side (e.g. 10B repack circuit 108 which receives the output of character synchronizing circuit 104 and reconstructs the characters; see page 17, bottom full paragraph).

VI. Differences over the prior art disclosed in the present application

Similar to the prior art disclosed in the present application, the data code is encoded as a predetermined length of bits (e.g., 10 bits for a data code encoded in the encoder 110). However, contrary to the Office Action the encoder 110 does not determine whether one of a plurality of control codes is present in a serial signal received from a transmission path. In both the disclosed prior art and claimed invention, the transmission path is at the side of the optical fiber interface 102. Also, unlike the prior art disclosed in the present application, the claimed control codes are of a smaller number of bits than the data code (e.g., 5 bits per control code vs 10 bits per data code).

Thus, unlike the disclosed prior art, the transmission device of the present invention comprises a determining means to inspect a bit string in groups the size of the second bit length (i.e., time to perform "character synchronization" is based on the second bit length) in order to determine whether one of the control codes is present in a serial signal received on the serial transmission path (i.e., time to perform "control code determination" is based on the second bit length), and sending means for determining the control code to be sent based on a result of the determination of said determining means, and sending the bit string containing at least the control code to be sent onto the serial transmission path (i.e., time to perform "control code addition" is based on the second bit length).

By having control codes with a smaller number of bits than the data codes, transmission delay time caused by control codes is reduced compared to conventional serial communication devices. In particular, the time required for "character synchronization", "control code addition"

and "control code determination" is reduced. (*Specification at page 21, lines 6-29*). This argument applies to independent claims 1, 7 and 13, as well as the respective dependent claims.

Applicants submit that the disclosed prior art and Walker, either alone or in combination, fail to teach each and every claimed element. Applicants request reconsideration and withdrawal of the rejection.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

CONCLUSION

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and such allowance is respectfully solicited. Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No. 48,222), to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1. 17; particularly, extension of time fees.

Respectfully submitted,

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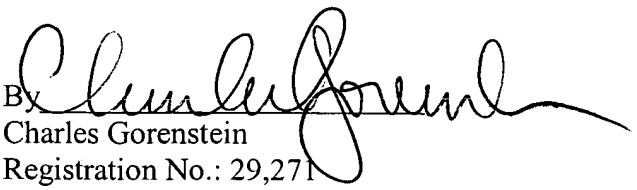
By 

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